



UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/621,185	07/15/2003	Sang-Deok Kim	51876P361	2348
8791	7590	10/12/2004	EXAMINER	
BLAKELY SOKOLOFF TAYLOR & ZAFMAN 12400 WILSHIRE BOULEVARD SEVENTH FLOOR LOS ANGELES, CA 90025-1030			KENNEDY, JENNIFER M	
			ART UNIT	PAPER NUMBER
			2812	

DATE MAILED: 10/12/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Advisory Action

Application No.

10/621,185

Applicant(s)

KIM, SANG-DEOK

Examiner

Jennifer M. Kennedy

Art Unit

2812

--The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

THE REPLY FILED 21 September 2004 FAILS TO PLACE THIS APPLICATION IN CONDITION FOR ALLOWANCE. Therefore, further action by the applicant is required to avoid abandonment of this application. A proper reply to a final rejection under 37 CFR 1.113 may only be either: (1) a timely filed amendment which places the application in condition for allowance; (2) a timely filed Notice of Appeal (with appeal fee); or (3) a timely filed Request for Continued Examination (RCE) in compliance with 37 CFR 1.114.

PERIOD FOR REPLY [check either a) or b)]

- a) ☒ The period for reply expires 3 months from the mailing date of the final rejection.
- b) ☐ The period for reply expires on: (1) the mailing date of this Advisory Action, or (2) the date set forth in the final rejection, whichever is later. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of the final rejection. ONLY CHECK THIS BOX WHEN THE FIRST REPLY WAS FILED WITHIN TWO MONTHS OF THE FINAL REJECTION. See MPEP 706.07(f).

Extensions of time may be obtained under 37 CFR 1.136(a). The date on which the petition under 37 CFR 1.136(a) and the appropriate extension fee have been filed is the date for purposes of determining the period of extension and the corresponding amount of the fee. The appropriate extension fee under 37 CFR 1.17(a) is calculated from: (1) the expiration date of the shortened statutory period for reply originally set in the final Office action; or (2) as set forth in (b) above, if checked. Any reply received by the Office later than three months after the mailing date of the final rejection, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

1. ☐ A Notice of Appeal was filed on _____. Appellant's Brief must be filed within the period set forth in 37 CFR 1.192(a), or any extension thereof (37 CFR 1.191(d)), to avoid dismissal of the appeal.
2. ☒ The proposed amendment(s) will not be entered because:
- (a) ☐ they raise new issues that would require further consideration and/or search (see NOTE below);
- (b) ☐ they raise the issue of new matter (see Note below);
- (c) ☒ they are not deemed to place the application in better form for appeal by materially reducing or simplifying the issues for appeal; and/or
- (d) ☐ they present additional claims without canceling a corresponding number of finally rejected claims.

NOTE: _____

3. ☐ Applicant's reply has overcome the following rejection(s): _____.
4. ☐ Newly proposed or amended claim(s) _____ would be allowable if submitted in a separate, timely filed amendment canceling the non-allowable claim(s).
5. ☒ The a) ☐ affidavit, b) ☐ exhibit, or c) ☒ request for reconsideration has been considered but does NOT place the application in condition for allowance because: see continuation sheet.
6. ☐ The affidavit or exhibit will NOT be considered because it is not directed SOLELY to issues which were newly raised by the Examiner in the final rejection.
7. ☒ For purposes of Appeal, the proposed amendment(s) a) ☒ will not be entered or b) ☐ will be entered and an explanation of how the new or amended claims would be rejected is provided below or appended.

The status of the claim(s) is (or will be) as follows:

Claim(s) allowed: _____

Claim(s) objected to: _____

Claim(s) rejected: 1,3 and 4.

Claim(s) withdrawn from consideration: _____


8. ☐ The drawing correction filed on _____ is a) ☐ approved or b) ☐ disapproved by the Examiner.
9. ☐ Note the attached Information Disclosure Statement(s) (PTO-1449) Paper No(s). _____
10. ☐ Other: _____



In response to applicant's argument that the references fail to show certain features of applicant's invention, it is noted that the features upon which applicant relies (i.e., controlling the etch ratio of the sacrificial layer by varying the process conditions such as RF power O₂ flow and a spacing between the substrate and the shower head) are not recited in the rejected claim(s). Although the claims are interpreted in light of the specification, limitations from the specification are not read into the claims. See *In re Van Geuns*, 988 F.2d 1181, 26 USPQ2d 1057 (Fed. Cir. 1993).

The examiner notes that the claim only recites the limitation that the sacrificial layer is formed in response to a RF power, an O₂ flow, and a spacing between the substrate and the shower head. The claim does not require that the etching ratio is changed according to these conditions. The examiner notes that Mozumder et al. was relied upon to show that the method forming a TEOS layer (the material of the sacrificial layer) is formed in response to a RF power, an O₂ flow, and a spacing between the substrate and the shower head (see column 4, lines 20-35).

Further, the examiner provided motivation to combine stating that it would have been obvious to one of ordinary skill in the art at the time the invention was made to form the TEOS sacrificial layer of the combined Ooto et al. and Cho by the method of Mozumder et al. by controlling the RF power, the O₂ flow, and the spacing between the substrate and the shower head in order to allow for optimal settings that allow for a uniform deposition rate of TEOS across the wafer and generally meet the tight set of specifications that integrated circuits require (see column 1, lines 25-35, column 2, lines 8-15, and column 4, lines 18-36).


John F. Niebling
Supervisory Patent Examiner
Technology Center 2800